Real time simulation of power electronics systems

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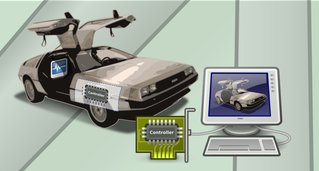
Background

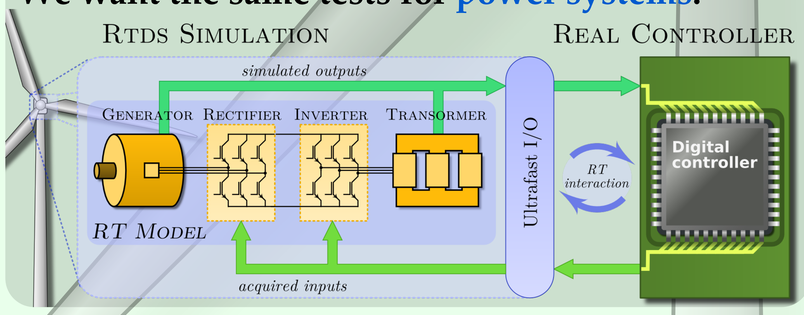
Hardware In the Loop (HIL)

System controllers require *extensive testing* to improve their reliability. However, it's often expensive or impossible to cover all the possible operating points and fault conditions.
Hardware In the Loop testing : the controller is *plugged into* a real-time (RT) simulator.

HIL tests already exist in the automotive industry for mechanichal systems



We want the same tests for power systems:



Our design

Provide a *flexible and easy to use platform* that supports a wide range of RT simulations of Power Electronics Systems, such as: wind turbines, electric cars, hybrid-electric cars, etc.
Our simulation runs at the electronic switch level, and can model all possible failure modes.

Benefits

Time-step: 500 ns

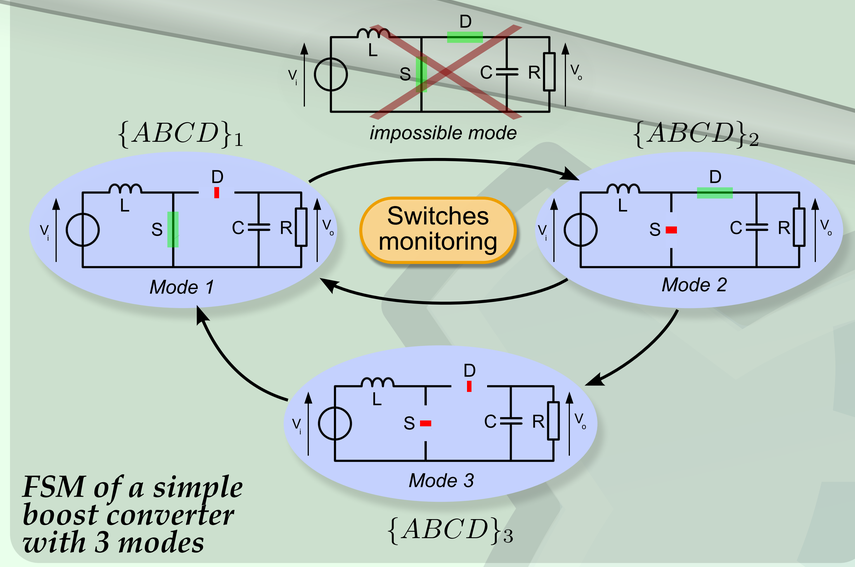
The Real Time Digital Simulation (RTDS) platform enables fully automated *testing* and *verification* of control hardware and software in power electronics.

Software tool architechture

Finite State Machine (FSM) design

The FSM description enables deterministic time computation

real-time algorithm



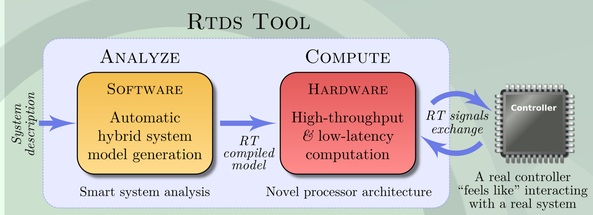
FSM of a simple boost converter with 3 modes

Key algorithm features

+ *Hybrid system* modeling approach
+ Continuous run vs. "single shot" analysis
+ Deterministic execution time algorithms vs. usual iterative ones
+ Ideal switch models vs. stiff snubbers (Lon, Ron)

General architechture

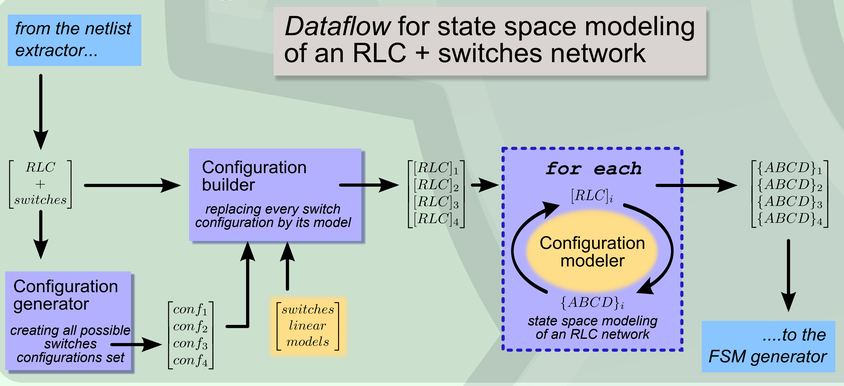
RTDS performance is based on a *double optimization*:
* Optimized circuit modeling
* Optimized computing platform



Circuit modeling

We simulate switched RLC networks:
These are *piecewise linear* systems.
* linear network: State space model
* switching: Finite State Machine (FSM)

Generating modes model



Creating the FSM description requires generation of all possible modes.
Then an *extensive topological analysis* of each circuit mode follows:
* Detect impossible modes
* Jump over metastable modes